Temperature Dependence of Spatially Resolved Picosecond Laser Induced Transients in a Deep Submicron CMOS Inverter

Jamie S. Laird, Yuan Chen, Tuan Vo, Larry Edmonds, Leif Scheick, and Philippe Adell

***Abstract*—Spatially-resolved picosecond laser induced transients have been measured in a 0.18 μm CMOS inverter test structure as a function of temperature. Sensitive n-drain and p-drain nodes have been scaled in size to accommodate characteristic differences between ion and laser tracks. Images based on pulse characteristics have been collected from 325 K to 400 K and transient currents extracted from laser strikes to both the OFF drain and its surroundings. With increasing temperature strikes to the OFF drain result in a pulse width which appears to broadens whilst the charge collected surprisingly decreases.**

***Index Terms*—CMOS devices, ionizing radiation, lasers, microwave circuits, space radiation effects, temperature effects.**

I. Introduction

AGGRESSIVE scaling leading to deep-submicron CMOS technology has resulted in Digital Single Event Transients (DSET) becoming a serious concern in determining upset rates in advanced combinatorial logic devices to be used in space [1]–[7]. A large factor in determining DSET propagation is the initial transient pulse shape [7] which depends on several factors including device structure, surrounding electrical network, as well as the ion track geometry and injection density via Space-Charge Screening Effects (SCSE) [8]. To date, most work investigating DSET generation in deep-submicron CMOS makes use of custom designed structures involving chains of inverters. Inverters are ideal since a hit to the reverse biased drain of an OFF transistor will always propagate above the threshold Linear Energy Transfer (LET) [6]. However, these custom devices do not necessarily represent packing densities in real devices; they are therefore unlikely to result in significant static temperatures due to accumulated ohmic losses. For drift and diffusion related charge collection at the high-injection levels present in an ion induced plasma, the relationship between temperature and pulse shape is potentially complex. Since temperature influences pulse shape, it should be considered an important variable to be logged like any other parameter.

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J. S. Laird is with the Jet Propulsion Laboratory, California Institute of Technology, Pasadena, CA 91109 USA, and also with the Commonwealth Scientific and Industrial Research Organization, Division of Exploration and Mining, School of Physics, University of Melbourne, Parkville 3052, Victoria, Australia.

Y. Chen, T. Vo, L. Edmonds, L. Scheick, and P. Adell are with the Jet Propulsion Laboratory, California Institute of Technology, Pasadena, CA 91109 USA.

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The aim of the work presented here is to experimentally measure transient currents in a custom designed 180-nm CMOS inverter to verify whether higher temperatures lead to pulse shape lengthening which to 1st order might be expected to result in a higher chance of DSET propagation. Using these results as a guide should allows one to extrapolate the likely response to higher and lower temperatures assuming simple mobility and diffusion length calculations (not performed here though).

The influence of temperature on heavy-ion induced transient current generation in bulk Si structures has been studied in the past. At low to cryogenic temperatures, increased acoustic mobility decreases pulse width in drift dominated charge collection [9]. Guo *et al.* measured the transient response at higher temperatures where pulse widths increase for both drift *and* diffusion dominated charge collection [10]. That being the case, it stands to reason that increased pulse widths at higher temperatures can be expected to result in a higher DSET propagation cross-section. Truyen *et al.* have in fact simulated DSET generation and propagation in the ATMEL 180 nm process from approximately 200 K to 400 K using 3D TCAD simulation [11]. In that work, DSET cross-sections did indeed increase several fold at higher temperatures.

In this work we use the JPL laser system for all analyses on the grounds that temperature related work can often be quite challenging and limiting in the range of LETs available [13]. In particular we use a spatially resolved picosecond laser and wide bandwidth sampling to directly measure transient currents ranging from 325 K–400 K. This regime corresponds to typical junction temperatures in real devices. However, one issue that needs resolving is whether a diffraction-limited laser strike, which basically covers an entire MOSFET, does in some way accurately simulate the average or most probable strike of an ion hitting all locations within the beam area i.e., is the laser induced transient a reasonable representation of the ion event leading to DSET propagation. Furthermore, since we eventually aim to correlate laser and ion results on the same device, the importance of correctly bounding the injected charge density is very important since both drift and diffusion processes are injection dependent [8], [14]. A typical inverter design was therefore "scaled up", and an optical port fabricated over central PMOS and NMOS drains to facilitate laser probing without interference from secondary effects such as losses due to metallization and diffraction at edges: both of which complicate any effective LET. Note this paper will *not* cover any MeV ion microbeam results.

II. Contribution to Pulse Width From Carrier Drift and Diffusion

A. Diffusion Controlled Drift Transport

Although diffusion is typically the rate limiting step for collecting charge in epilayer junctions, high-injection SCSE are known to result in ambipolar diffusion controlled drift in the Quasi-Neutral Region (QNR) of the ion track [8]. These screening effects lengthen the pulse width by a degree which depends on device structure, track characteristics and minority carrier diffusivity [7], [15]. Understanding the relative roles of drift and diffusion in determining the pulse shape is important if the effect of temperature on pulse width is to be properly understood. According to Edmonds theory on these matters, the charge collected during the SCSE phase is:

$$Q^{a}_{n,p}(t) = \frac{\alpha D_{p,n}}{D_a} Q_0 G\left(D_a t/\gamma z_s^2\right) \tag{1}$$

where α and γ are constants depending on the epilayer structure ($\alpha = 2, \gamma = 4$ for a p^+-n-n^+ and $\alpha = \gamma = 1$ for an n^+-p-p^+ junction), $D_{n,p,a}$ are the electron, hole and ambipolar diffusivities (cm^{-2}/s), Q_0 is the charge injected, and the function G is given by:

$$G(\zeta) = 1 - \frac{8}{\pi^2} \sum_{i=0}^{\infty} (2i+1)^{-2} \exp[-(2i+1)^2 \pi^2 \zeta] \tag{2}$$

where z_s is the time-dependent width of the QNR [8]. Recent analyses on the MeV ion induced response of p^+-n-n^+ junctions noted excellent fitting using the Edmonds model over the 100–300 K region [16]. For this work, extending the model from 300 K to 400 K is assumed reasonable given the lower carrier mobilities and longer screening periods further re-reinforce its basic tenets. According to (1), the rate of charge collection is largely controlled by the QNR width which depends on the technology node in question.

B. Case for CMOS Inverter

For the CMOS inverter structure used here, the maximum possible screened plasma length is much less than the 5–10 μm range studied in previous p^+n-n^+ diodes. According to Mavis *et al.*, the collection depth in similar 180 nm structures is $\sim$1 μm i.e., the maximum possible QNR is $\sim$1 μm. This translates into a zeroth order solution (the longest duration component in the Fourier series shown in (2)) at least 100 times faster than the 1–2 ns observed in the p^+-n-n^+ Si diodes discussed above [15], [17]. For the n^+ p structures found in the NMOS regions, the ambipolar period of charge collection is even faster due to the higher minority carrier diffusivity (electrons). Hence for both HIGH and LOW inputs on the inverter structure, pulse widths are likely to be dominated by diffusion. Benedetto *et al.* observed heavy-ion induced pulse widths in 180 nm bulk CMOS to be between 1–2 ns depending on applied bias [3], [18]. This fact further suggests diffusion from below and lateral to the collecting drain is responsible for observed pulse widths. With this being the case, the geometrical relationship between the plasma track and collecting node becomes more important.

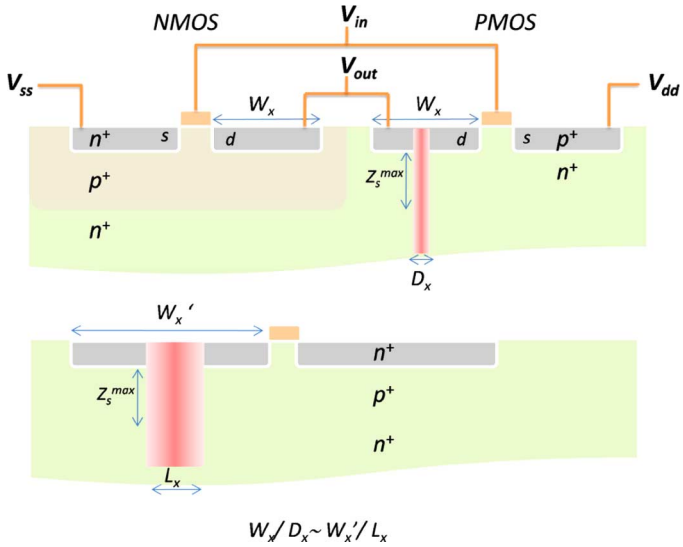

Fig. 1. (Top) Cross-sectional view of a CMOS inverter struck by an ion with a thermalised carrier distribution of width D_x (FWHM). (Bottom) The same PMOS region scaled up to cope with a diffraction limited laser pulse with a diameter L_x (FWHM). Importantly, in both cases the maximum QNR width has the same value of $Z_s^{\max}$ independent of drain size for vertical ion strikes. Note the struck component is the same as measured experimentally.

C. Scaled Design for Accurate Diffusion Contribution

For reasons already pointed out, typical sub-micron drain and source dimensions have been scaled to 5 × 5 μm to accommodate laser probing with 1–2 μm beams. The effect of nodal scaling is summarized in Fig. 1 for an ion and laser induced plasma of diameters D_x and L_x, respectively. Most importantly, the scaling leads to a ratio W_x/D_x which is very close to W_x'/L_x, meaning charge collected by diffusion is similar if high-injection effects such as the density dependent lifetime can be ignored. Furthermore, scaling justifies the boundary conditions, required by the derivation of (1) for both cases. The two arrangements are similar from the point of view of charge collection by diffusion, and will produce similar charge-collection rates. These assumptions will of course fail as technology scales to the level where $W_x \rightarrow D_x$ and complex device architecture dictates the exact role of diffusion. However, for the purpose of the structures used in this paper, the above scaling approximation is probably reasonable and the key point to derive from it is that diffusion related charge collection is probably similar between the laser in the scaled n^+p diffusion and an ion in a normal size cell. Another advantage of these test structures is that optical windows over the n-drain and p-drain's allows one to investigate transient formation from strikes on the respective OFF drain, as well as those due to proximity strikes by hits in the complimentary ON drain window i.e., the role of lateral diffusion in determining pulse shape. Even though the structure is larger, its dopant-depth profile results in a QNR characteristic of the technology node in question.

One benefit of the larger structure (in conjunction with additions described later) is the ability to drive higher loads such as a low-impedance transmission line. This allows us to examine transients at higher bandwidths. One negative corollary however, is that output voltage transients from these inverters are not typical of the technology node as discussed later. Whilst these

voltage transients cannot provide a general rule of thumb for 180 nm technology, numerous other authors have already done this. Most recently, Ferlet-Cavrois *et al.* used a pulsed laser and impedance probe to measure voltage transients on the output of a chain of inverters at room temperature [19]. This work concentrates on current pulse widths as seen on the supply rails as a function of temperature.

D. Temperature Dependence of Ion and Photon-Generated Plasma

Beside the obvious difference in track widths for MeV ion and laser probing, fundamental differences between the photon-solid and ion-solid interaction is responsible for track differences with temperature [12]. Rapid thermalisation of an ion induced plasma predominantly occurs via Auger scattering and Longitudinal Optical (LO) phonon emission (Raman scattering) [20], [21]. Higher electron energies generated in the ion event preferentially scatter with LO, rather than acoustic phonons meaning track thermalisation is independent of temperature i.e., the track shape and density are almost solely determined by Band-Gap Narrowing (BGN) and its effect on the electron-hole pair creation energy [16]. Photons in the UV-infra-red range on the other hand, generate much cooler carriers by comparison and acoustic phonon scattering dominates. The phonon density-of-states *is* important and its decrease at lower temperatures leads to longer absorption lengths which alters the effect laser LET. In theory though, the temperature dependence of the absorption length can be compensated for by scanning wavelength as discussed elsewhere [12]. Unfortunately the method was not applied here and interpreting data is prone to systematic error.

A laser wavelength of 800 nm was chosen for all work presented here. As noted however, a serious complication with temperature analyses using picosecond lasers is the temperature dependent change in $1/\alpha$ and LET due to Band-Gap Narrowing (BGN) at higher temperatures [22]. Fortunately, the reflection coefficient from Si with a thin film of nitride of oxide is largely invariant with temperature. Likewise, the index of refraction for SiO_2 and Si_3N_4 is almost uniform from 500 nm to 1.5 μm at respective values of around 1.5 and 2.0 [23]. Using a well known absorption model at 800 nm [24], the absorption length $1/\alpha$ was estimated to vary from 7.8 μm at 325 K down to 5.8 μm at 400 K. The theoretical laser LET therefore increases by some 20–30%. Shown in Fig. 2 are estimated laser induced plasma profiles (in arbitrary units) for a 100 pJ $\lambda = 800$ nm beam focused to a 1.5 μm spot on Si held at three of the temperatures used in this work. These volumes have been estimated using the method outlined by Melinger *et al.* [25]. The higher LET at 400 K introduces *some* systematic error into quantitative comparisons, which can be partially compensated for by modelling.

III. Experimental

A. Device Under Test

The 180 nm CMOS test structure was fabricated at TSMC using the MOSIS service and contains numerous devices including the single inverter used here. The single inverter structure is illustrated in Fig. 3. In the center of the photograph are

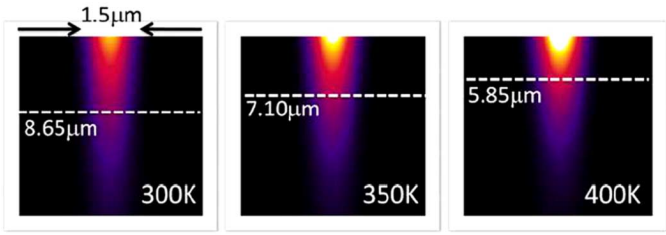

Fig. 2. Calculated carrier distribution profiles (arbitrary units) for an 800 nm 100 pJ laser pulse focused onto Si for the temperature range investigated here.

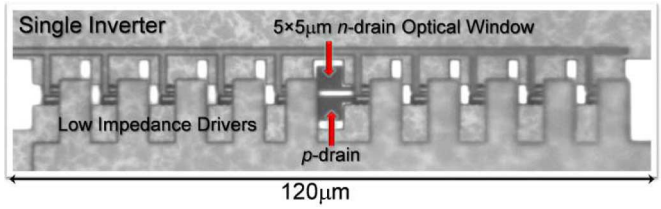

Fig. 3. (Top) Optical photomicrograph of the 120 μm long inverter fabricated for spatially-resolved transient current experiments as a function of temperature. The 5×5 μm optical drains are shown in the middle.

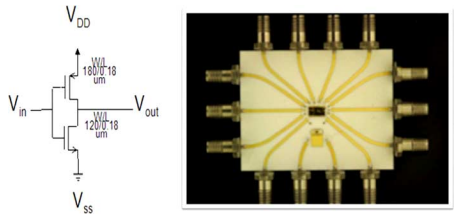

Fig. 4. Circuit diagram for the single inverter chain including PMOS ($W/L = 180/0.18$ μm) (top) and NMOS ($W/L = 120/0.18$ μm) (bottom) FETs with widths W and lengths, L. (Right) Custom designed 26 GHz carrier with 50 Ω transmission lines. A Si p-i-n diode mounted below the CMOS test structure is used for various laser tests.

the 5×5 μm optical drains. The typical supply voltage $V_{\rm dd}$ is 1.8 V but rated up to approximately 2.5 V. Unlike previous research where specialized latches or DICE circuits indirectly monitored DSET propagation [2]–[4], here we use a scaled transistor with parallel CMOS components designed to drive a 50 Ω low-impedance line. The parallel PMOS and NMOS regions (shown to either side of the optical drains) reduce the effective "on resistance" by orders of magnitude (kΩ's to Ω's). Devices were mounted on the ceramic carrier with multi-SMK connections shown in Fig. 4 (right) [12]. This carrier mounts into a modified Linkam microscope cryogenic stage for temperature control from $\sim$80 K to $\sim$450 K.

External wide bandwidth bias tees commonly used for these types of experiments [26], [27] were mounted on the air side of the Linkam stage. The role of bias-tees is to maintain a constant supply voltage at both rails so that the ensuing AC coupled transient recorded on a DSO is simply that due to a current swing at the device node [28], [29]. In practice the magnitude of the voltage swing on the output is of more interest since this determines the likelihood of propagation [30]. At 1.8 V, the $V_{\rm dd}$ supply current was 28 mA giving a series resistance of 12.5 Ω. The series resistance of each bias tees is 5.6 Ω which accounts for 90% of the observed value.

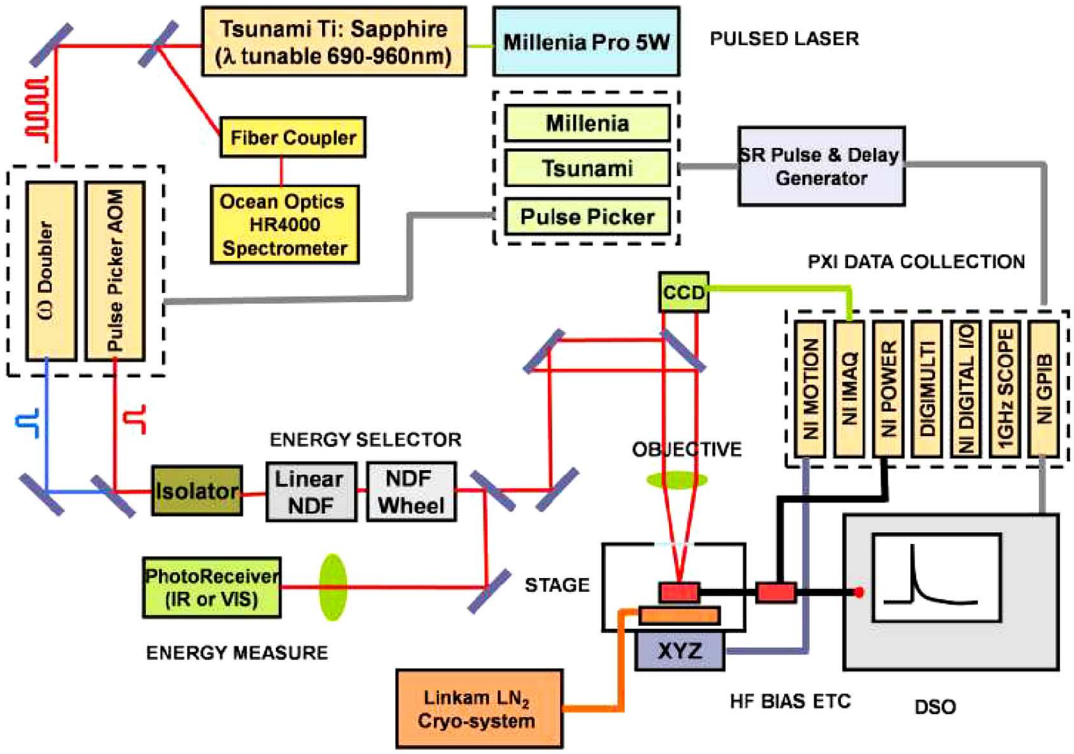

Fig. 5. Schematic of the JPL laser system configured for cryogenic to high temperature analysis of high-speed SEE phenomenon [12].

B. Picosecond Laser System for Temperature Analyses

The JPL scanning picosecond laser system was used for all measurements discussed in this paper. A schematic of the system in its configuration for high-speed transient measurements with temperature is given in Fig. 5. The system is similar to the IXL system, at the Université Bordeaux, France [31]–[33]. At the center of the system is a tunable Spectra-Physics Ti: sapphire mode-locked Tsunami laser pumped by a 5 W Millennia Pro5s laser at 532 nm (frequency doubled from Nd: YAG diodes). The Tsunami cavity is mode-locked at 80 MHz and tunable over a broad range from 690–960 nm. The Pulse Picking Unit (PPU) is controlled by a Stanford Research pulser in combination with timing derived from the laser clock train: it typically runs from Hz to several kHz. Neutral density filters (NDF) are available for attenuation: one a linear design with a 0–100% transmission range and the other, a filter wheel for more specific optical densities (0.01–3OD). Calibrated photo-receivers (New Focus) for the near IR (model-1623) and visible (model-1621) regime indicate energy stability typically varies over 5–10%.

A vertical periscope comprising two mirrors aligns the beam onto the input port of a vertical microscope. An input diaphragm is used to further limit beam divergence entering the microscope optics. A turret including a series of long working distance Olympus lenses are available ($\times 10, \times 50$ and $\times 100$) depending on required spot size and depth of field. A CCD camera feed coupled with stage software (see later) can be used to position the laser spot or scan it between fiducial points. The camera can also be used to correct for any thermal expansion in the beam axis using the automated *XYZ* stage to maintain focus at the same position. Maintaining focus is critical as spot size not only determines image resolution but the transient current pulse shape in some device structures [15], [17]. Average laser energy and LET are measured using a Thorlabs (PM-100 and S130A detector) mounted at a fiducial point on the sample stage. Energies per pulse typically range from 1 pJ to 1 nJ at the DUT. For this work a 20 ± 1 pJ beam was used for all temperatures giving theoretical effective LET values in Si of $\sim$51 and 75 MeV/mg/cm^{-2} at 300 K and 400 K, respectively. Note that these LET values have not been inferred by comparison with ion results and are only meant as a rough guide for a *likely* upper limit.

C. Transient Measurements

All of the data collected here was done with $V_{\rm gs}$ tied HIGH i.e., the output $V_{\rm out}$ was driven low making the PMOSFET OFF with its p-drain becoming the largest SET sensitive volume. Under this condition, the transient current is largely dictated by hole collection via diffusion from the substrate. Guesstimates predict a slower transient in this instance. For all measurements, a 20 pJ 800 nm laser spot was raster scanned across a 60 μm $\times$ 20 μm central region of the inverter structure incorporating both NMOS and PMOS regions, and all three signals ($V_{\rm ss}, V_{\rm dd}$ and $V_{\rm out}$) were simultaneously recorded on a 6 GHz DSO. The DSO was pre-triggered using a signal derived from the PPU. As with the Benedetto *et al.* study on a similar 180 nm TSMC process, the bias $V_{\rm dd}$ was initially ranged from 1.1 V to 2.5 V at 325 K to investigate the effect of current starving on the shape of the transient current [18] and to allow comparison with previous authors results on the same 180 nm technology node.

Scanned data over the same region was then collected in 25 K steps from 325 K to 400 K for several $V_{\rm dd}$ values. Only tran-

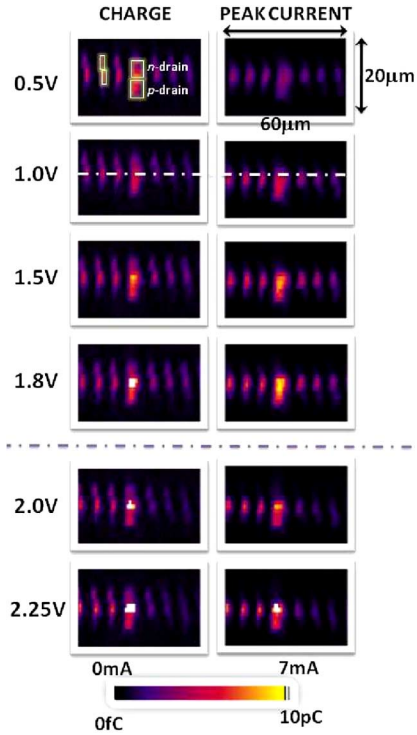

Fig. 6. Bias dependence of the charge and peak current of the transient response measured on V_{ss} to a 20 pJ laser pulse scanned across the optical drain and 6 neighboring MOSFET groups. The set temperature was 325 K and λ was 800 nm.

sients collected on $V_{\rm dd}$ and $V_{\rm ss}$ with $V_{\rm gs}$ tied HIGH will be shown in this paper since an unfortunate side-effect of the design is that a single ion strike, whilst collapsing the struck node, cannot dissipate charge stored on the parallel nodes driving the higher load. The resultant voltage swing as measured by $V_{\rm out}$ does not fall into a complete ON/OFF state thereby complicating analysis with circuit effects. In fact, the device has been hardened against transient propagation. However, the current transient on $V_{\rm dd}/V_{\rm ss}$ and their respective pulse shape characteristics are still representative of nodal collapse on the drain being probed. Any lengthening of the transient current on $V_{\rm ss}$, for example, will result in a longer DSET on $V_{\rm out}$ although the response due to re-charging of nodal capacitance may differ.

IV. Results

A. SET Imaging

Images based on transient characteristics such as total charge, peak current and rise/fall times can be derived by Pulse Shape Analysis (PSA) on the 60 μm $\times$ 20 μm multi-dimensional $(n+2)$D data-set $[x, y, i_0(t) \ldots i_n(t)]$. Example images for the case of transients taken on $V_{\rm ss}$ at 325 K as a function of bias are shown in Fig. 6. For orientation with the design mask, an overlay of the p-drain (bottom) and n-drain (top) dimensions is given on the top left charge image

Besides the gap region between optical drains where a large current exists for $V_{\rm dd}$ beyond 1.8 V, the largest transient response occurs for strikes to the OFF p-drain as measured on $V_{\rm ss}$. This was not unexpected since the NFET is ON (its $V_{\rm gs}$-V_t is equal to $V_{\rm dd}$-V_t which is positive). The term V_t is the threshold

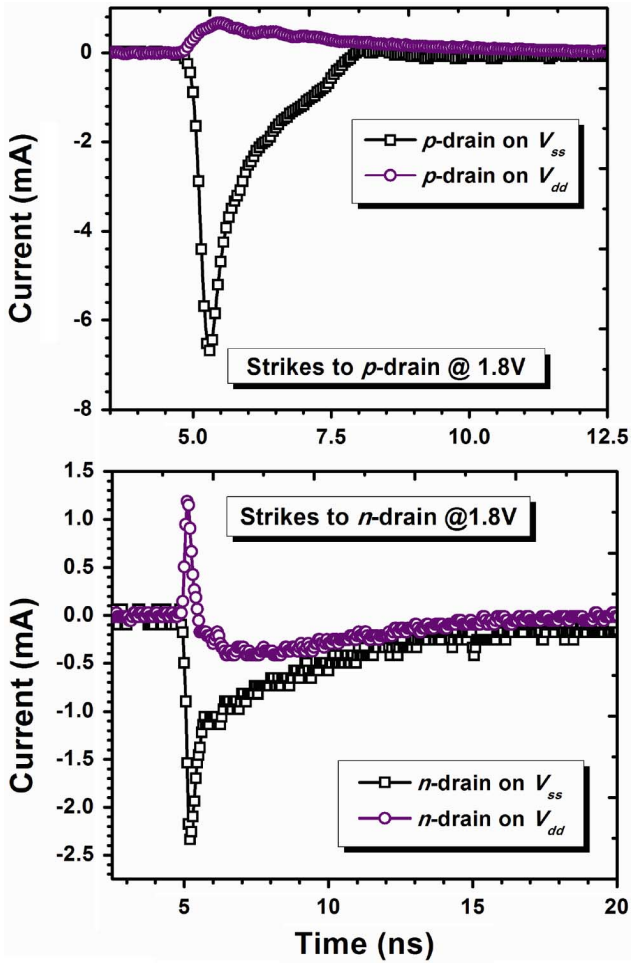

Fig. 7. (Top) p-drain and (Bottom) n-drain transients collected on $V_{\rm dd}$ and $V_{\rm ss}$ at 325 K for the case of 1.8 V. The p-drain transient on $V_{\rm ss}$ represents the largest charge collection transient but not the longest transient in the system.

voltage. Since the sensitive PFET in Fig. 1 is OFF, the lowest impedance path resulting in a large signal is via $V_{\rm ss}$ to ground (the serial ON NFET has a relatively low resistance). Transients generated on $V_{\rm ss}$ are therefore more relevant for DSET propagation for a HIGH input. For brevity, analyses of images collected on $V_{\rm dd}$ are not shown here.

Interestingly, the response in the gap region is highly temperature and bias-dependent, hinting at a parasitic charge collection path that may be interfere with the ability to discern simple charge collection mechanisms'. Above $V_{\rm dd} = 1.8$ V, the charge and peak current response in the neighboring MOSFETs appears to decrease, possibly in relation to a bipolar/latching/shorting action in the gap. Strikes to this spot were avoided in analysis. Given that a certain fraction of charge generated in strikes to either drain can diffuse to the gap, some small level of contamination may exist for strikes some distance from the gap.

A relative measure of the importance of $V_{\rm dd}$ and $V_{\rm ss}$ transients seen from a peak height and width perspective is given in Fig. 7. This figure illustrates typical pulses collected on $V_{\rm dd}$ and $V_{\rm ss}$ for strikes on the middle of the p-drain (Top) and n-drain (Bottom). Although strikes to the n-drain are markedly longer, their heights are 3–4 times smaller than p-drain transients on

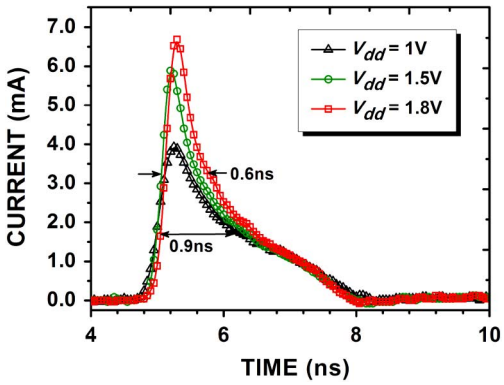

Fig. 8. Bias dependence of p-drain transients on $V_{\rm ss}$ at 325 K illustrating a pulse width which increases from 0.6 ns to 0.9 ns (truncates after ~3 ns). Small structure after this point may be recharging of the node capacitance [11].

$V_{\rm dd}$. The bipolar response for strikes to n-drain measured on $V_{\rm dd}$ is may be related to displacement current induction due to capacitive coupling [34]. Henceforth only $V_{\rm ss}$ transients are discussed and their sign is *inverted* for convenience.

B. Bias Dependence of $V_{\rm ss}$ Transients

The above data-sets can be sectioned to extract assorted information. For example, shown in Fig. 8 are the $V_{\rm ss}$ current transients collected for direct hits on the p-drain as a function of bias from 1 V to 1.8 V at 325 K. Benedetto *et al.* reported DSET pulse widths ranging from around 0.3 ns to 1.5 ns in 180 nm CMOS for ion LETs greater than 80 MeVcm^2/mg [2]. In another paper it was reported that DSET pulse widths depend primarily on supply voltage $V_{\rm dd}$ [18]. Transient widths as defined by the Full Width at Half Maximum (FWHM) range from 0.6 to 0.9 ns from 1 V to 1.8 V (since the output voltage remains collapsed for a good fraction of the complete pulse, this definition of pulse width may not be an appropriate measure) [7]. Note the slightly negative region after the transient tail is the point where the node capacitance is recharging i.e., the output voltage is being restored. This point appears to be independent of bias.

C. Temperature Dependence of $V_{\rm ss}$ Transients

Shown in Fig. 9 are the same images collected from 325 K to 400 K for the typical operating point of $V_{\rm dd} = 1.8$ V. Fall-times images (scale of 0–6 ns) have also been included to illustrate the longest transients (also the smallest) come from the n-drain regions. Shown in Fig. 10 are $V_{\rm ss}$ transients for laser strikes on the p-drain collected at 1.0 and 1.8 V as a function of temperature. These were extracted from the middle of the p-drain images shown in Fig. 9.

The scale for each transient has been normalized by the ratio of the theoretical laser LET at each temperature to that calculated at 325 K i.e., a factor of $\sim 75/56$ for the 400 K case. As mentioned earlier, this scaling law assumes a charge collecting depth much less than several absorption lengths, which is true according to the Mavis data discussed earlier.

Shown in Fig. 11 are the charge transients (left-bottom) estimated by integrating the currents in Fig. 10. Also shown is the asymptotic charge collected divided by the effective laser LET at all temperatures, as well as a polynomial fit. From 325 K to

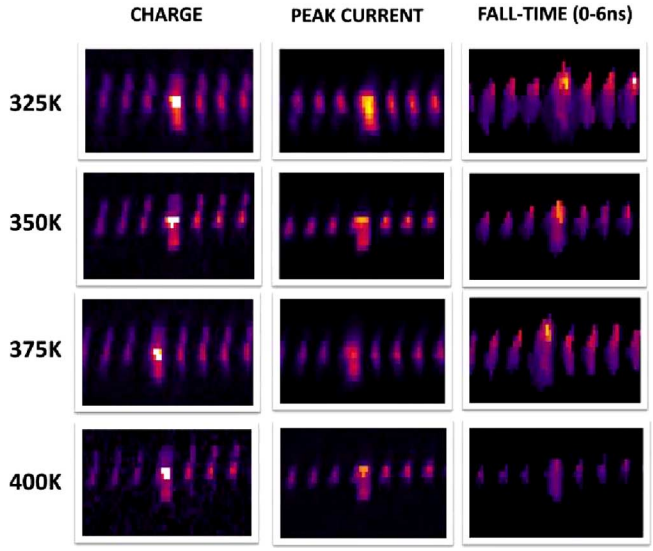

Fig. 9. Charge and peak current images of the inverter structure collected using a 20 pJ laser pulse scanned across the optical drains and 6 neighboring MOSFET groups. The bias $V_{\rm dd}$ was 1.8 V and the temperature scanned from 325 K to 400 K in 25 K steps. The laser λ was 800 nm. Images of the transient fall-time (0–6 ns on the same color scale given in Fig. 6) indicate the region around the n-drain to give the longest pulse.

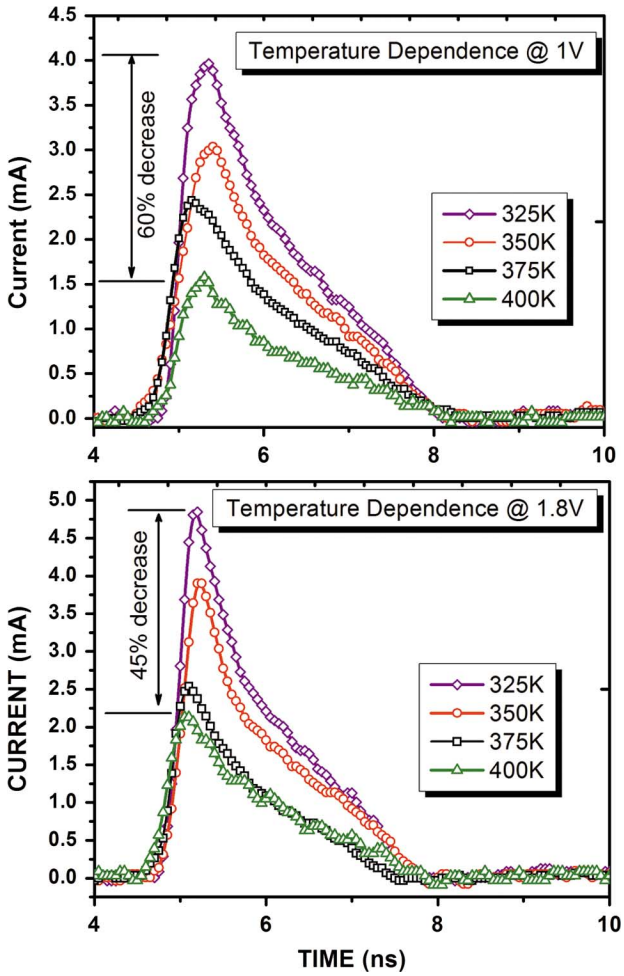

Fig. 10. Temperature dependence of $V_{\rm ss}$ p-drain transients measured at $V_{\rm dd} =$ 1 V (Top) and 1.8 V (Bottom) from 325 K to 400 K. Scaling factors have been applied to normalize the 325 K data.

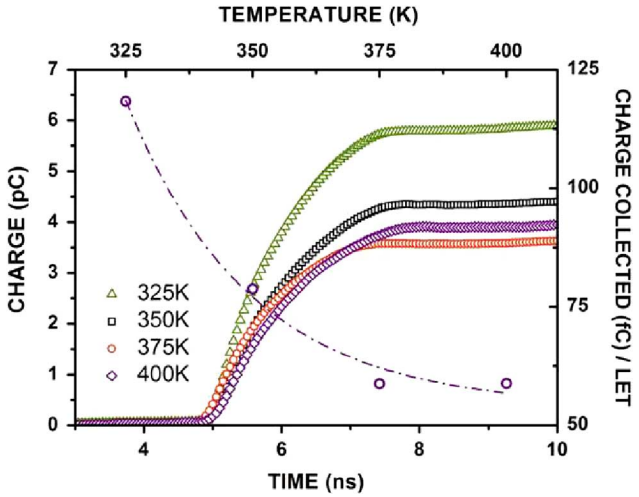

Fig. 11. (Right-Bottom) Charge transients on V_{ss} indicates the rate of charge collection is similar for all temperatures. Normalizing each transient to its maximum results in almost perfect overlap for all transients suggesting the only quantity changing is the injected charge.

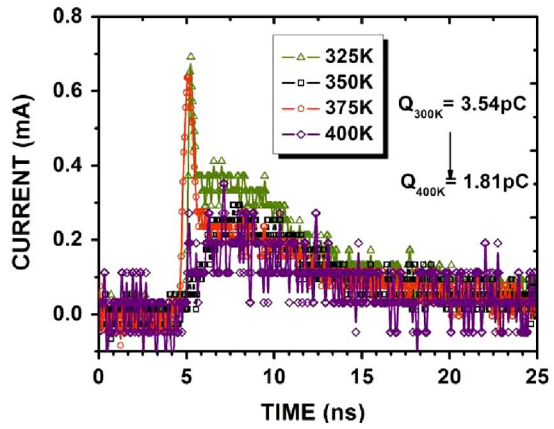

Fig. 12. Transient currents measured at V_{ss} for strikes to the ON n-drain transistor (roughly midway) for all four temperatures indicating a decreased diffusion current at higher temperatures.

400 K, the charge decreases by some 30% which is surprising given effective laser LET has increased by a similar measure.

D. Diffusion Transients From Strikes Away From p-Drain

Since charge collection for strikes to the OFF drain is collected by a combination of drift and diffusion, it is interesting to view transient data collected from those lateral to this point. Here, strikes to the center of the n-drain (ON transistor) are used since this area has the same geometrical window size and optical transmission. Shown in Fig. 12 are these set of data indicating charge almost halves from 3.54 pC to 1.81 pC over the same temperature range (integrated charge transients are not shown for brevity). The data is considerably noisier due to the significantly smaller amplitude; spatial averaging could not be performed since pixel-to-pixel variation in the signal can result in relatively large errors of around 20% or so.

V. Discussion

For the case of direct hits to the OFF p-drain, the peak current due to ambipolar-drift transport in the junction decreases as predicted by (1). The total drop in both charge and peak current (including normalization) is as large as 45% or so at 1.8 V. At lower biases this loss increases out to 60% at 1.0 V). A total charge decreasing strongly with temperature was not observed by Guo *et al.*, although the substrate doping of around 4×10^{15} cm^{-3} [10] used there is probably quite different to that used here (judging by the relative collection lengths). The qualitative trend observed in our data also disagrees with that of Truyen *et al.* [11] and does in fact suggest a marked drop in minority carrier diffusion length at higher temperatures, which did actually occur in the Guo *et al.* data, but to a much reduced extent.

Since the duration of any SCSE if considerably shorter than 1 ns in the p-drain, most of the observed width (and charge) is due to slower diffusion from the p^+ tub or n^+ substrate. This is primarily due to the known decrease in carrier mobilities at higher temperatures which decreases carrier diffusivity. The Dorkel and Leturq mobility model in Si predict a 400 K electron and hole diffusivity $D_{n,p}$ of 22.0 and 7.4 cm^2/s which increases to 28.2 and 8.8 cm^2/s from 300 K to 400 K (this is for a guess doping level of 10^{16} cm^{-3} in the p^+ substrate). If one assumes diffusion length L_d to go as $\sqrt{D_{n,p}\tau_{n,p}}$, then a constant temperature in-dependent lifetime $\tau_{n,p}$ results in a 12% drop in charge collected by diffusion. This increases to 25% for a doping of 10^{14} cm^{-3} which an unlikely scenario since a drift collection length of close to 10 μm would result. Since the charge collected (normalized to the average LET) almost halves from 325 K to 400 K, we suspect a significant recombination term and/or a large systematic error. The most obvious form of error may be associated with the laser LET normalization process. However, similar experiments on a simple n^+ p structure fabricated on the same CMOS test chip display a similar temperature dependence, even after adjusting the wavelength to correct for the temperature dependent absorption length [12]. Likewise, those particular structures were very simple meaning circuit effects can be discounted as a source of systematic error (although they still might affect the overall pulse shape). We believe the effects measured here to be real and the shape to be approximately correct.

The above increase in losses are most likely due to recombination in the plasma track, in part exacerbated by the increased duration of high-injection SCSE at higher temperatures [9], [10]. Longer collection periods leads to larger Auger scattering losses [8], [35]. However, the still short-lived SCSE suggests a significant reduction in the high-injection lifetime due to the dense plasma produced by each laser pulse. Previous analyses on a Si p-i-n structure using an even longer wavelength (at much reduced energies of around 1 pJ) noted Auger losses of the order of a few percent within a fully depleted device [36]. The order of magnitude larger energies applied here, combined with the shorter wavelength means carriers densities are at least several orders of magnitude higher. Since the Auger lifetime $\tau_{\rm aug}$ is inversely quadratic with injection level [37], a significant portion of the losses reported here *may* be ascribed to Auger recombination. The increasing Auger recombination coefficient at higher temperatures [38] also results in a higher loss. According to Svantesson *et al.* the Auger coefficient increases from around 3.9×10^{-31} cm^6 s^{-1} at 294 K to 4.6×10^{-31} cm^6

s^{-1} at 372 K (similar to the range considered here). This factor alone represents a 15% decrease in collected charge.

It is interesting to note that Guo *et al.* did not observe significant Auger losses like those postulated here even though the ion tracks used there would have resulted in higher carrier densities.

A noteworthy fact is that the dominance of diffusion in these devices means the use of custom CMOS test structures (for reasons already explained) may have played an important role. In theory data could be extracted from the smaller neighboring sites for comparison. However, the response from these areas is only several pixels wide and large variations in response were observed as shown in Figs. 6 and 9. This variation means the normalization procedure used to correct for temperature variations in the laser LET may amplify this variation making general trends more difficult to observe. The gap region has however been an unfortunate oversight in design.

VI. Conclusion

SET imaging of a deep-submicron CMOS inverter structure results in a complex spatial relationship between pulse height, total charge and fall-times as seen for data collected on both rails. Current transient shapes for strikes in and lateral to the OFF p-drain vary substantially at higher temperatures. This is primarily due to decreased mobilities and diffusivities at higher temperatures leading to slower charge collection and higher recombination losses. Although temperature was expected to increase pulse width, the large loss in charge due to Auger scattering tended to mask the affect. According to these results, one might expect DSET issues to reduce at higher temperatures in this technology node. However, due to complexities in the device response, more work may be needed to clarify several points raised. We believe the data to be a useful discussion point for future experiments.

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